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Processing-Enhanced SEU Tolerance in High Density SRAMs

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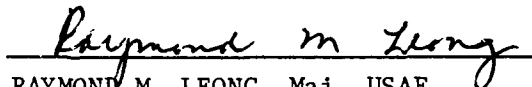
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We report theoretical calculations and experimental verification of an increase in memory cell SEU tolerance when Sandia's 2-μm-technology 16K SRAMs are fabricated with a radiation-hardened 1-μm CMOS process. An advanced two-dimensional transient transport-plus-circuit simulator has been employed to calculate the differential contributions from each of the vertical dimensional changes in the transition from the 2-μm process to the 1-μm process. Error cross-section data, performed at the Berkeley cyclotron on the first such device lot, indicate that total improvement in threshold LET is a factor of 2 or better. A saturation phenomenon associated with the high-LET events is described, and physical mechanisms responsible for the saturation are discussed.

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FIGURES

TABLE

I. INTRODUCTION

It is well known that increasing the CMOS SRAM tracking densities decreases its SEU tolerance levels.[1-4] The general trend of process evolution to accommodate such lateral dimensional miniaturization is to increase the doping concentration, decrease the oxide thickness, and have twin and/or retrograde tubs on a very thin epitaxial substrate. These process modifications increase the specific capacitances (the junction and gate capacitances per unit area) and reduce funneling collection of ionization-generated charges. Consequently, a memory cell's intrinsic SEU tolerance is enhanced for equivalent design geometries of the active elements.

We would, therefore, expect an increase in SEU tolerance when Sandia's 2-μm technology 16K SRAM (SA3240) could be fabricated with a 1-μm (as opposed to a 2-μm) process. Physical realization of such a hybrid chip is accomplished by the use of a newly developed radiation-hardened 1-μm process[5] to fabricate Sandia's TA670, which is a 2-μm 16K SRAM design with the same cell geometry as the SA3240 for the metal interconnects.

Comparisons of SEU data between TA670 and SA3240 thus provide the total combined effects of all the processing changes from the 2-μm process to the 1-μm process. To determine the effects of an individual process change by actual process splits in a fabrication lot is simply not cost-effective. We, therefore, resort to Sandia's advanced simulator for transient SEU logic simulations to rank-order the individual importance of each processing change in the transition from the 2-μm process to the 1-μm process.

The simulator has been experimentally verified with SEU tolerance levels of the resistively hardened 16K SRAM SA3240 over a large range of LET events. We find the simulator also satisfactory for predicting the SEU tolerance of chips fabricated with the 1-μm process. Both experimental and simulated SEU tolerance levels of TA670 are compared with those of SA3240. A saturation phenomenon associated with high-LET events involving very heavy ions is described, and the physical mechanisms responsible for the saturation are discussed.

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II. SEU EXPERIMENTS

The first hybrid chip lot of TA670 yielded memories with decoupling resistance ~100 kΩ. The heavy ion experiments at Berkeley showed that, for normal 5-V and room-temperature operations, the threshold LET of TA670 is about twice that of its counterpart SA3240 chips also having R_{dc} = 100 kΩ (Fig. 1). For krypton ions angled at 60 deg (LET ~80 MeV-cm^2/mg), these 100-kΩ TA670 chips will behave very much like SA3240 chips having 200 kΩ on the feedback links. This means that 100 kΩ TA670 chips under the normal operating conditions described above will have an error rate less than 1×10^{-10} errors/(bit-day) for Adam's 10% worst-case galactic environment.[6] Figure 2 shows that the threshold LET of 205 kΩ SA3240 is lower than the threshold LET of 100 kΩ TA670 for a reduced supply voltage and elevated temperature operations. The reduction of the decoupling resistance at elevated temperatures for TA670 is less than that for SA3240 because lower-valued resistors have lower thermal coefficients of resistivity, which are normally proportional to the total number of impurities contained in the resistor. A very thin polysilicon process, which is much less sensitive to temperature variations, is currently being developed at AT&T Bell Laboratories.
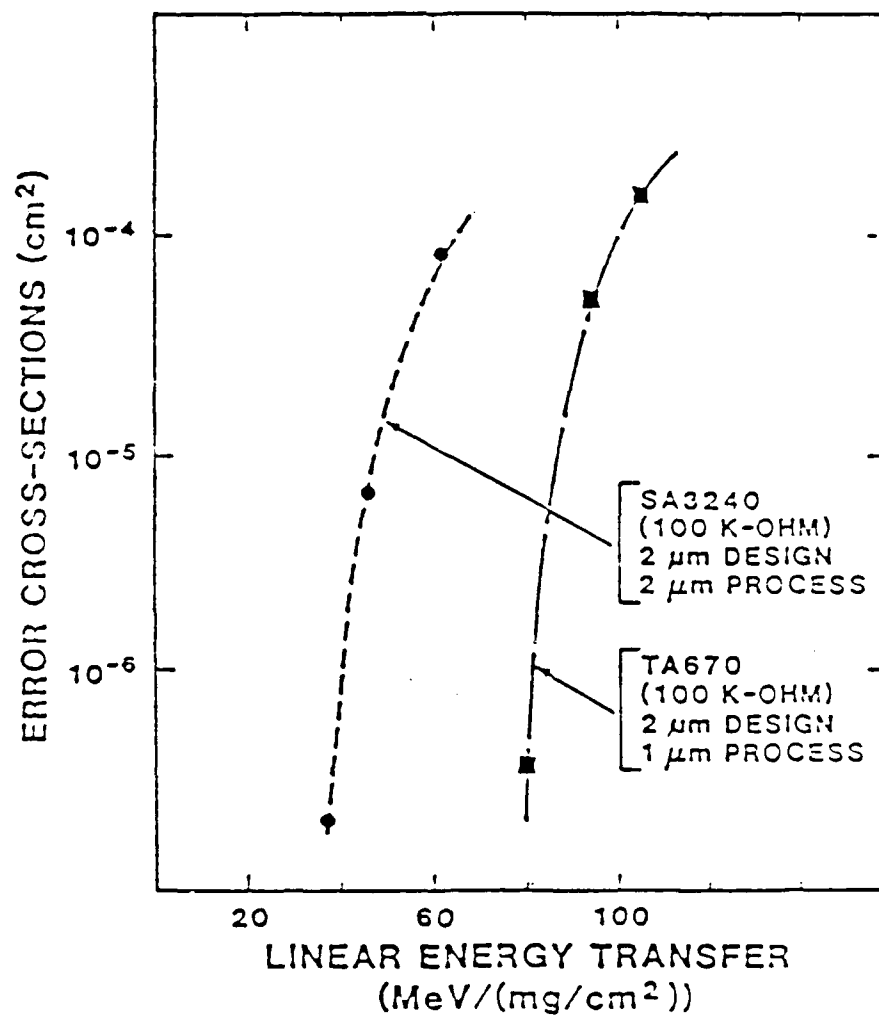
Fig. 1. Error Cross Sections of SA3240 and TA670 Hardened
with 100 kΩ Resistors on Their Feedback Links for
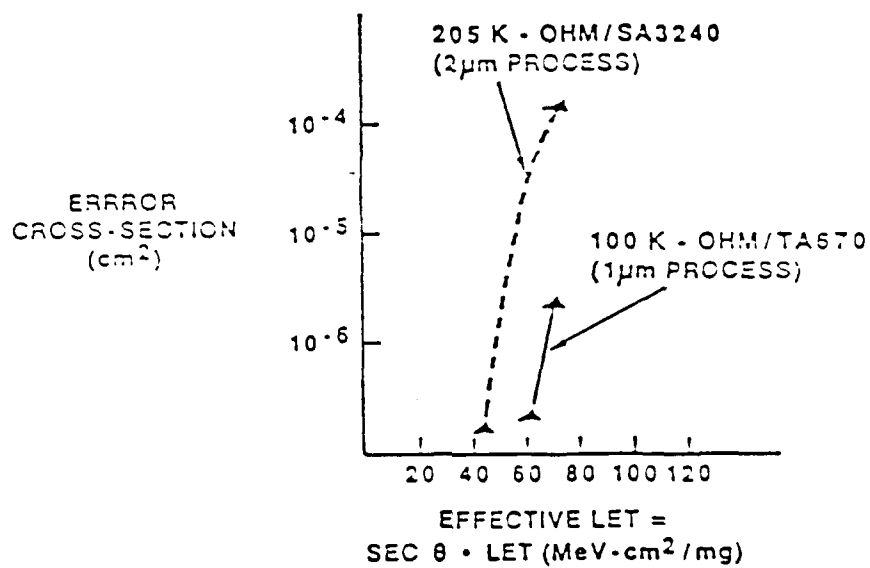Operation at Room Temperature and 5 V

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Fig. 2.   Error Cross Sections of SA3240 and TA670 Hardened,
          Respectively, with 100 and 205 kΩ Resistors on
          Their Feedpack Links for Operation at 50°C and 4.5 V

III.   THE SIMULATION MODEL

Sandia's SEU simulations consisted of solving the five semiconductor
equations for the four individual FETs of the cross-coupled inverters
(Fig. 3). The two-dimensional doping profiles for SA3240 were formed from the
spreading resistance profiles as described earlier.[7] Device doping profiles
of TA670 (1-µm process) are generated by AT&T's BICEPS program. Table 1 lists
the important differences in vertical dimensions for these two processes. We
simulated each LET event on the most sensitive p-drain by the instantaneous
addition of a slab of electron-hold pairs of proper densities. The struck
p-drain voltage usually responds instantaneously from low to high and
eventually either recovers to low (cell not upset) or remains high (cell
upset). For the case of "cell not upset," we obtain the recovery time for the
given LET event.[8] Recovery time thus provides a measure of the duration of
the SEU-induced transient and is a quantitative indicator of the SEU
sensitivities.

In the case of "cell upset," the struck p-drain upset voltage stays high
and is transmitted to the unstruck node in the $R_{dc}C$, where C is the inverter
capacitance. We call this RC time, the decoupling time associated with the
decoupling resistor R_{dc}. When the decoupling resistor is large enough to
provide the decoupling time that is longer than the recovery time of a
specific LET event, the memory circuit is protected by R_{dc} against the
specific LET. Additionally, calculation of the decoupling time furnishes an
accurate calculation of the dynamic cell capacitance associated with the
specific voltage transition, which is much more realistic than the usual
static method of estimating capacitance with the crude depletion
approximation.

For low-LET events, such as α-particles, recovery time or cell sensitiv-
ity is directly proportional to the intrinsic charge-collection capability at
the struck junction. We would, therefore, expect enhanced SEU tolerance when
we increase the substrate doping density and reduce the epitaxial thickness by
the use of the 1-µm process. For high-LET events, the hole-collecting current

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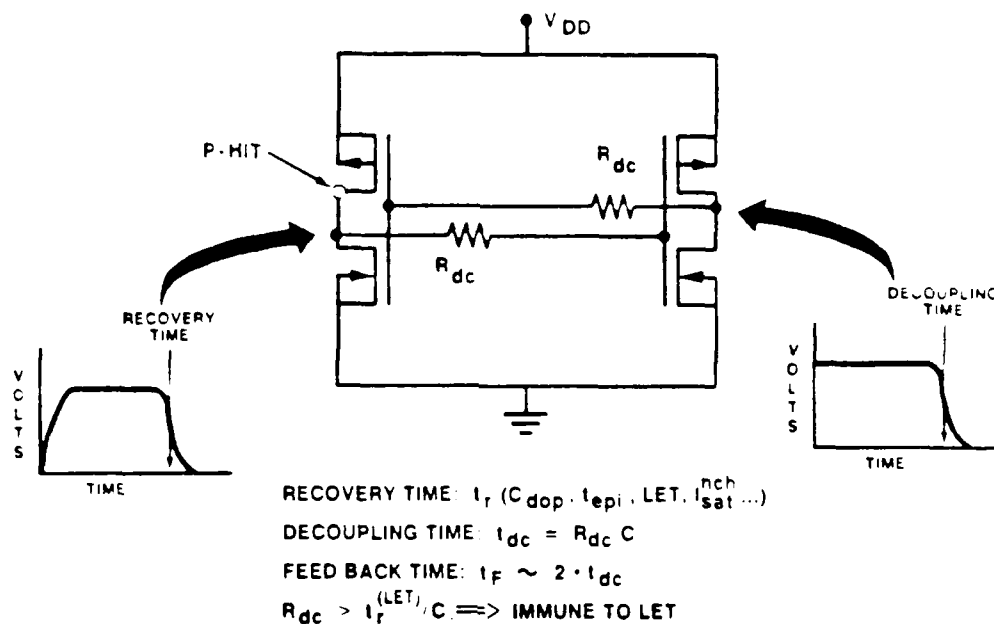
Fig. 3.   Schematic of the Resistively Hardened CMOS SRAM Cell without Its Two Pass Transistors. In our two-dimensional SEU simulations for the 16K SRAMS, SA32-0 and TA670, each FET is replaced with a slab of silicon represented by its proper source/drain, substrate doping profiles, and ohmic contacts generated for the 2- and 1-μm processes. We define the recovery time of a p-drain hit as the time at which the struck node switches from 0 to VDD and then comes back down to VDD/2. The decoupling time is defined as the time for the unstruck node voltage to decrease from VDD to VDD/2.

Table 1. Important Doping Profile and Vertical Dimensional
Differences between Sandia's 2-µm p-Well and AT&T
Bell Laboratories' 1-µm Twin-Tub CMOS Processes

	Sandia's 2-µm p-Well Process (SA3240)	AT&T-Bell Laboratories' 1-µm Twin-Tub Process (TA670)
Gate Oxide Thickness	300 Å	215 Å
N-Substrate Surface Doping	$4 \times 10^{15}/cm^3$	$5 \times 10^{16}/cm^3$
Epitaxial Substrate Thickness	3.0 µm	1.7 µm

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sourcing out of the p-drain is, however, limited by the conductance of the load device, i.e., the saturation current at the n-FET. Recovery time or cell sensitivity is then highly dependent on the current-carrying capability of the n-FET.[8]

IV. DISCUSSION OF RESULTS

The gate oxide thickness of the TA670 is about two-thirds that of the SA3240; its effective channel length is nearly 2 μm. However, the 2-μm process used to fabricate SA3240 over-etches in order to produce sloped polysilicon edges, resulting in an effective channel length of < 1.5 μm. The net result of these differences in processing details is that both SA3240 and TA670 provide about the same saturation current for the n-FETs at VD = VG = 5 V. Although the p-channel drain junctions of TA670 and SA3240 differ in their charge-collection capabilities, they are loaded with the same conductance to the ground. As we showed earlier, the intrinsic charge-collection capability at the struck junction is not detrimental to the recovery times of high-LET events; therefore, we conclude that TA670 and SA3240 may have similar recovery times for such high-LET events.

Figure 4 shows that the calculated recovery times for TA670 are slightly smaller than those of SA3240 in spite of the very thin epitaxial substrate and the high doping densities of the shallow n-tub. We conclude that recovery time or cell sensitivity following a p-drain hit is dominated by the conductance of the loading device connected to the struck junction.

Other evidence of the importance of this circuit-loading effect is the large increase in calculated recovery times for the modified TA670 simulations. Modified TA670 simulations use the same 1-μm doping profiles of TA670, except that the gate oxide thickness is 300 Å, not 215 Å. This leads us to expect identical charge-collection capabilities at the struck junctions of TA670 and the modified TA670. However, the conductance at the load n-FET of the modified TA670 has decreased by 30% from that of TA670 because of the increase in gate oxide thickness. The fact that recovery times of modified TA670 are longer than those of SA3240 or TA670 indicates that thinning epitaxial thickness and reducing funneling charge collection are ineffective methods for enhancing SEU tolerance of high-density CMOS SRAMs.

For effective SEU immunity to a given LET event, the decoupling resistor needs to provide a decoupling time that is longer than the recovery time of
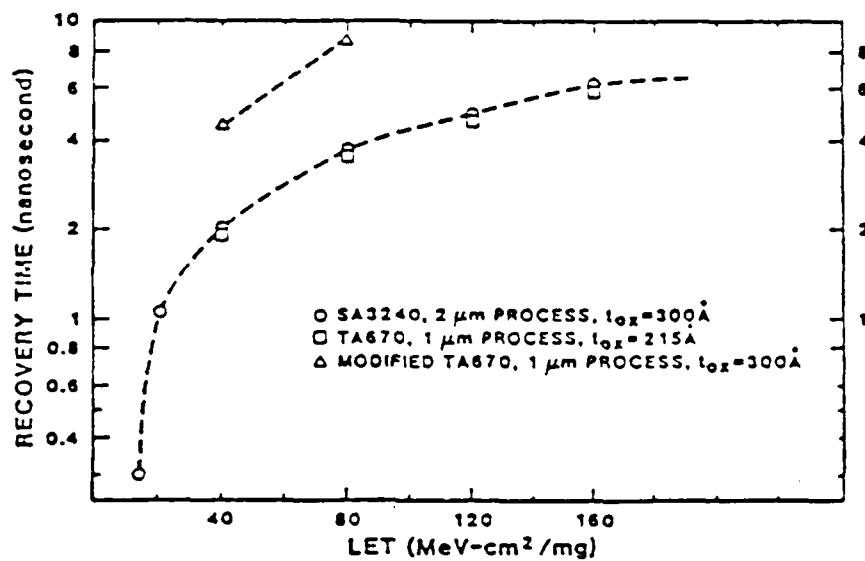
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Fig. 4. Simulated Recovery Times as a Function of LET for SA3240,
TA670, and the Modified TA670 with Thicker Gate Oxide.
For each given ion LET strike on a given memory cell
with a specific resistor, the simulation results in either
upset or recovery. We determine either decoupling time for
the "upset" case or the recovery time for the "not upset"
case.

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the corresponding LET (Fig. 3). Figure 5 shows that decoupling times of TA670 are much longer than those of its equivalent counterpart SA3240 (having the same resistances on the feedback links) because of the increased specific capacitance at the gate and the junctions. Consequently, relatively smaller resistance of TA670 provides the same protection as does a SA3240 chip with a larger decoupling resistor.

Figure 6 shows good agreement between the simulation results and experimentally determined threshold LETs as a function of energy deposition, for both SA3240 and TA670. The feedback, or decoupling, resistor values of Fig. 6 can also be interpreted as the critical or minimum resistor values required for SEU immunity to a specific ion LET event. SEU saturation phenomena are clearly evident in the rapid decrease in the required differential increase in these resistor values. Finally, no additional resistance is necessary as the LET becomes large. Thus the RC times associated with these resistors determine upper bounds to the durations of SEU-induced perturbations, which are represented by our simulation figure of merit, the recovery time. This means that as the LET increases, the recovery time increases with a decreasing slope and is finally bounded, as shown in Fig. 4.

The shape of this simulated recovery time is, however, quite different from our earlier calculations reported.[8] In these earlier calculations for SA3240, a low multiplicative factor (A = 100) on the Auger recombination coefficients was used for correcting the two-dimensional effect of artificial lowering of the LET-induced generation densities.[7] Figure 7 shows that, as the LET increases, the recovery time increases without bound for this insufficiently corrected low-recombination model while the saturation phenomenon is brought about by the high-recombination model (A = 1000). Most important, good agreement between the simulations and the experimental results shown in Fig. 6 can only be reached by this new high-recombination model.

This saturation phenomenon allows us to conclude that we don't need infinitely large resistors to provide SEU immunity against infinitely large LETs, because there exists a physical mechanism limiting the durations of the SEU-induced transients. This limiting mechanism increases with the increase
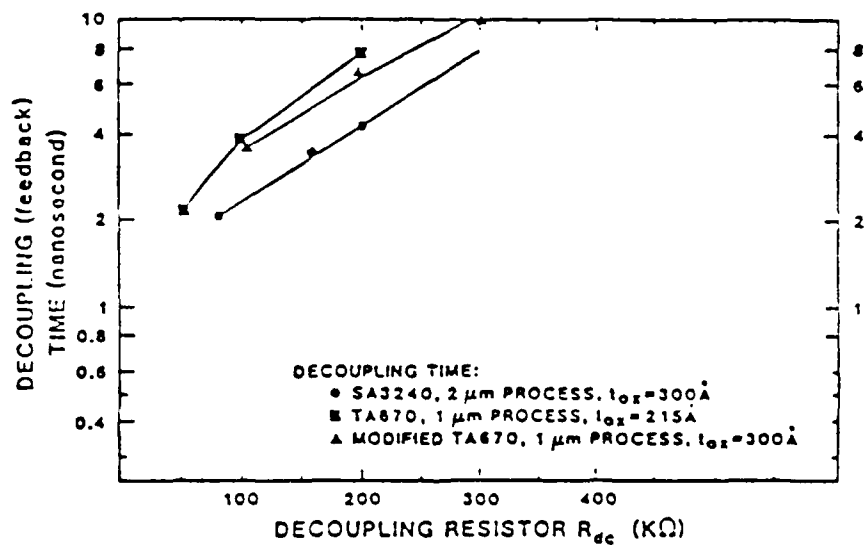
Fig. 5. Simulated Decoupling Times as a Function of LET for SA3240, TA670, and the Modified TA670 with Thicker Gate Oxide
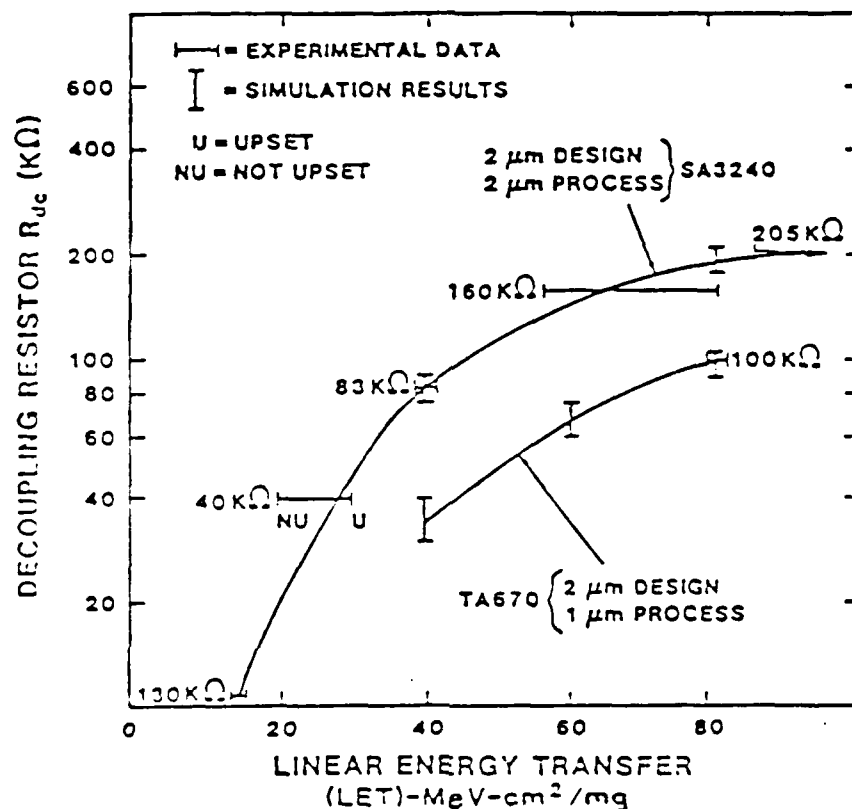
Fig. 6. Comparison of Experiments and Simulation Results.
The experimentally determined "upset" and "not upset"
LETs are shown as the right and left ends, respectively,
of the horizontal bars specified with the decoupling
(feedback) resistor value of the memory device. The
vertical bars depict simulation results of the specific
ion event that produces "upset" and "not upset," respec-
tively, for memories hardened with the top and the bottom
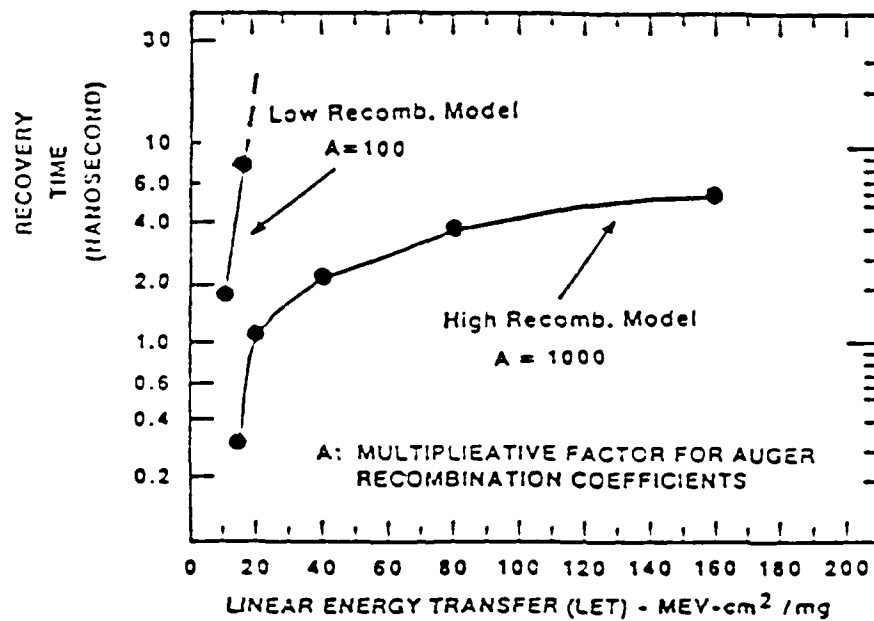resistances of the vertical bar.

Fig. 7. Recovery Times Calculated with Low- and High-Recombination
Models for p-Drain Events of SA3240. The experimentally
measured saturation current values of the load device
n-FET are used for both models.

of generation density and results in the self-termination of any additional LET threat. The critical variable responsible for this self-termination process is the rate of the Auger band-to-band recombinations of electrons and holes. The rate of this recombination becomes significant only when the carrier densities become very high.[9] Detailed analyses will appear in another publication.

Finally, we would like to note that this processing-enhanced SEU tolerance is not readily apparent when we observe that a 64K SRAM fabricated with a 1-μm technology is invariably much less SEU tolerant than a 16K SRAM chip fabricated with a 2-μm technology. The overall softness of the densely packed memory chips, which results from the reduction of SEU tolerance due to the size down-scaling, overshadows the aforementioned processing-enhancement effect. This miniaturization softening effect will be demonstrated by comparing the TA670 data with our new data from the test chip TC17. The memory chip TC17 contains 1024 bits of the prototype 1-μm CMOS SRAM, which will be used as the unit cell of our 256K SRAM design. The unit cell area of TC17 is 215 μm^2, which is only one-fifth the unit cell area of TA670 or SA3240. Comparison of the SEU data of the TC17- and the TA670-provided scaling effect derived solely from the lateral dimensional reductions, since both TC17 and TA670 were fabricated with the same 1-μm process.[5] A detailed discussion of the geometric scaling was reported at the 1987 International Electron Device Meeting in December in Washington, D.C.

V. CONCLUSIONS

We have demonstrated that 1-μm processes are inherently more SEU tolerant than 2-μm processes for a given CMOS static memory design, primarily because of the increased specific capacitance. The reduction of junction charge collection, achieved by thinning the epitaxial substrate and/or by raising the n-tub doping concentration, is of less significance. Following high-LET events, the induced-voltage transient pulse widths or the recovery times of a given memory cell design are dominated by the conductance of the loading device connected to the struck junction.

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